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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,715	01/13/2001	Hiroaki Tsugane	15.31/5631	2451

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[REDACTED] EXAMINER

MAGEE, THOMAS J

ART UNIT	PAPER NUMBER
	2811

DATE MAILED: 09/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/759,715	TSUGANE ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 02 June 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-4 and 15-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-4 and 15-29 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>14</u> .	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 15, 17, 18, and 23 – 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakoh (US 6,384,444 B2) in view of Owens et al. (US 4,598,460), Koo et al. (US 6,404,001 B2), Oji (US 5,420,449), and Richiuso (US 2001/0013632 A1).

3. Regarding Claims 1 and 15, Sakoh discloses a method for manufacturing a semiconductor device having a DRAM, including a cell capacitor (right side) (Figure 8) and a capacitor element (left side) formed in the analog region, whereby an impurity region in the DRAM region (3) is used to connect an electrode (14) of the capacitor. Sakoh does not disclose that an impurity region is present in the substrate to connect an electrode in the analog section. However, Koo et al. disclose (Col. 7, lines 17 – 21) that the embedded connection (14e) is in contact with a source/drain (impurity) region. Hence it would have been obvious to one of ordinary skill in the art at the time of the invention to use the impurity interconnect of Koo et al. to connect to the bottom electrode of the capacitor in the analog region of Sakoh.

Sakoh further discloses (Figure 8) that the dielectric layer (12) of the cell capacitor and the

capacitor element are formed simultaneously and in like fashion, the cell plate (19) of the cell capacitor and the upper electrode of the capacitor element are also formed simultaneously. Koo et al. disclose the simultaneous formation of lower electrode layer (16) (Figure 1), dielectric layer (17) and upper electrode (18) to form capacitors (Figure 2) in the cell array and peripheral regions (Col. 5 line 66 through Col. 6, line 2). Additionally, Oji discloses (Col. 2, line 52 through Col. 3, line 6) the formation of a capacitor with bottom and top polysilicon electrodes (4,6) (Figure 1) and an insulating film (5) in the flash memory section that can be also formed (simultaneously) in other portions of the device. Further, Richiuso discloses that capacitors (C1 – C6) can be formed simultaneously in different physical locations within the circuit Figure 2), wherein a polysilicon layer forms bottom electrode (40(a)) with an insulating layer and an electrode atop.

Sakoh does not disclose the simultaneous formation of the ion implanted impurity regions in the analog and memory region, however, the simultaneous doping of separate device regions by ion implantation is conventional (See Owens et al., Col. 8, lines 14 – 16) and utilized for more than two decades. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to perform simultaneous doping of the regions to reduce the number of processing steps.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Owens et al.,Richiuso, Oji, Koo et al., and Sakoh to form a completed functioning device having DRAM and analog regions.

4. Regarding Claim 17, Sakoh discloses the formation of a semiconductor device

including a DRAM region and an analog region with capacitors formed in each region (Figure 8) wherein an interlayer dielectric layer (6,16) formed on the semiconductor substrate where the dielectric is between the substrate and capacitor. Sakoh does not disclose the formation of an impurity region in the analog region whereby the embedded connection layer contacts the impurity region. However, Koo et al. disclose (Col. 7, lines 17 – 21) that the embedded connection (14e) is in contact with a source/drain region. Hence it would have been obvious to one of ordinary skill in the art at the time of the invention to use the impurity interconnect of Koo et al. to connect to the bottom electrode of the capacitor in the analog region of Sakoh.

5. Regarding Claim 18, Sakoh does not disclose the formation of an additional capacitor element and an additional embedded connection layer where the layer extends from the additional capacitor to the impurity region and serial connection of the two capacitors is provided through the impurity region. Koo et al. disclose (Col.7, lines 6 – 8) that the lower capacitor electrode (16a) is connected to an impurity source/drain region through interconnect, 14a. It would have been obvious to connect capacitor lower electrodes in the analog region to impurity regions in the substrate and to combine Sakoh with Koo et al.

6. Regarding Claims 23 - 26, Sakoh does not disclose the thicknesses of dielectric layers, but the capacitor insulating layers are approximately equal in thickness, as shown in Figure 8.

7. Regarding Claim 27, Sakoh disclose forming an additional capacitor in the DRAM

region (far right, Figure 8)

8. Regarding Claim 28, Sakoh does not disclose the simultaneous formation of the ion implanted impurity regions in the analog and memory regions. However, the simultaneous doping of separate device regions by ion implantation is conventional (See Owens et al., Col. 8, lines 14 – 16) and utilized for more than two decades. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to perform simultaneous doping of the regions to reduce the number of processing steps.

9. Regarding Claim 29, Sakoh discloses simultaneously forming the storage node of the cell capacitor (Figure 8) and the additional storage node (26) of the additional cell capacitor, simultaneously forming the lower electrode of the capacitor element and additional capacitor element (Figure 8), simultaneously forming the dielectric layer of the cell capacitor (18) and the dielectric layer (18) of the additional cell capacitor, simultaneously forming the dielectric layer (18) of the capacitor element and the additional capacitor element, simultaneously forming the cell plate of the cell capacitor and additional cell capacitor, and simultaneously forming the upper electrode of the capacitor element and additional capacitor element (19).

10. Claims 2 – 4, 16, and 19 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakoh in view of Owens et al., Koo et al., Oji, and Richiuso, as applied to Claims 1,15,17,18, and 23 – 29 above, and further in view of Choi et al. (US 6,040,596).

11. Regarding Claims 2, 3, 16, 19, and 20, Sakoh does not disclose the formation of resistance elements in the analog region. Choi et al. disclose the fabrication of a device with DRAM and peripheral circuit regions containing capacitors and resistors in the analog region. Choi et al. disclose the formation of a first and second resistance element (Figure 5A), where the sheet resistance of the two is adjusted by varying the impurity concentration introduced into the polysilicon (Col.5, lines 62 – 65). It would have been obvious to one of ordinary skill in the art at the time of the invention to alter the relative impurity concentrations of the two resistance elements to produce a lower resistance in the first element, since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Nagai further discloses that the cell plate of the capacitor (38) and the electrode of the resistor (38) are the same and hence are formed simultaneously (Col. 5, lines 45 – 50).

It would have also been obvious to one of ordinary skill in the art at the time of the invention to combine Choi et al. with Sakoh to obtain resistance elements in the analog region in order to complete the analog circuit for a functioning device.

12. Regarding Claims 4, 21 and 22, Sakoh does not disclose the formation of resistors or the use of silicide layers. Choi et al. disclose (Figure 1B) the formation of a silicide layer (29b) on the polysilicon layer (29a) of the resistor. Since the resistance of the polycide layer is lower than that of the polysilicon (Col. lines 56 – 65), it would have been obvious to one of ordinary skill in the art at the time of the invention to deploy a polycide in the first resistance element to produce a low sheet resistance value relative to the second.

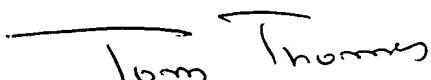
Response to Arguments

13. Applicant's arguments have been carefully considered but are regarded as moot in terms of the new ground(s) of rejection. In regard to Applicant's interpretation of Choi (p. 4), Applicant is in error and has misinterpreted the intent of Choi. It would be illogical to modify the resistors to have equal resistance values after they have been separately doped to different concentrations. Choi discloses (Col. 3, lines 57 – 60) that it is the large variations or anomalies within an individual resistor (essentially a quality control issue) that will require adjustments, not adjustments to make resistors of the same sheet resistance. They are usually never of the same resistance, even when done by design.

Conclusions

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396**. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722**.

Thomas Magee
August 23, 2003


TOM THOMAS
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